REMARKS

Claims 1-42 are pending in this application. In the Office Action dated December 21, 2004, the Examiner took the following action: (1) objected to the title as being non-descriptive; (2) rejected claims 5 and 6 under 35 U.S.C. § 112, second paragraph, as failing to point out and distinctly claim the subject matter; (3) rejected claims 1-5, 7-12, 14-19, 21, 29-33, 35-40 and 42 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,525,988 to Ryu *et al.*; and (4) rejected claims 6, 13, 20, 22-28, 34 and 41 under 35 U.S.C. § 103(a) as being unpatentable over the patent to Ryu *et al.*, in view of what was well known in the art.

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed embodiments of the invention are a system and method for reducing the power consumed by a delay-locked loop ("DLL") when a device, such as a memory device, transitions from an active mode to an inactive mode. As explained in the "Background" section of the application, it is conventional to disable a DLL by locking its delay interval when a device containing the DLL transitions to an inactive mode. As a result, when the device transitions to an active mode, the DLL can more quickly achieve a locked condition.

The disclosed examples of the invention are directed to solving a somewhat subtle problem that can be encountered when using the above-described technique to lock the delay interval of a DLL when transitioning from an active mode to an inactive mode. As also described in the application in which a memory device is used as an example, a memory device transitions to an inactive mode in response to a memory command. However, operating conditions of the memory device can be disturbed as a result of the memory device responding to the memory command. For example, the memory device may draw additional power in responding to the memory command, which can decrease internal power supply voltages. If the delay interval of the DLL is locked before the operating condition has stabilized, the delay interval of the DLL may be affected by the instability. As a result, the DLL may have the incorrect delay interval when the memory device transitions back to an active mode. The disclosed examples of the invention address this problem by not simply locking the delay interval of the DLL upon detecting a transition to an inactive period in which the DLL is not needed. Instead, the disclosed method and system also detects when the device is stable after reacting to a command applied to the device. Only then, after the device has stabilized, is the delay interval of the DLL locked.

The primary reference cited in the Office Action is the patent to Ryu *et al.*, which discloses a system for activating a DLL when a memory device containing the DLL transitions from a first inactive mode, *i.e.* a self-refresh mode, to a second inactive mode, *i.e.*, a standby mode. In such case, the DLL is activated for either a predetermined period of time or a predetermined number of clock cycles. Unlike applicant's disclosed system, the system disclosed in Ryu *et al.* involves controlling the DLL when a memory device transitions from one inactive mode (in which the DLL is not needed) to a second inactive mode (in which the DLL is also not needed). More specifically, when transitioning from one inactive mode to the next, the Ryu *et al.* system activates the DLL for a predetermined period of time or number of clock cycles. In contrast, applicant's disclosed system relates to controlling a DLL when transitioning from an active mode (in which the operation of the DLL *is* needed) to an inactive mode (in which the operation of the DLL is not needed).

According to the Office Action, Ryu *et al.* teach in column 1, lines 56-58 and column 2, lines 13-15 "a device inactive decoder providing a device inactive signal when the DLL need not continue adjusting a delay interval to synchronize with the system clock." However, that is not what is described in the cited portions of the Ryu *et al.* patent or anywhere else therein. Instead, the cited portion of the Ryu *et al.* patent states "a control circuit activates the delay locked loop circuit for a predetermined time when the semiconductor memory device transitions from a self refresh mode, in which the DLL circuit is deactivated, to a standby mode." [Column 2, lines 12-15]. In the standby mode, the DLL is, of course, also not needed. Therefore, as explained above, what Ryu *et al.* teach is briefly activating the DLL for short period when transitioning from one inactive mode to another inactive mode. The Ryu *et al.*

patent does not teach any circuit that generates a signal when transitioning from an active mode in which the DLL is needed to an inactive mode in which the DLL is not needed.

The Office Action also states that the Ryu *et al.* patent discloses in column 4, lines 29-35 "a stabilization detection device [fig. 1] providing a stabilization signal when the device is stable after reacting to a command applied to the device." To the contrary, what is stated in the cited text is "[t]he PSELF signal indicates whether the DRAM is in self refresh mode and, thus, may be used to indicate when the DRAM has transitioned from the self refresh mode into a standby mode. The PDLLCNT signal is disabled (deactivated) a predetermined time, such as a selected number of clock cycles, after the transition to a standby mode." Therefore, the quoted section of the Ryu *et al.* patent again simply describes generating the PSELF signal to activate the DLL when transitioning from the self refresh mode to the standby mode, and then disabling the PDLLCNT signal to the activate the DLL after a predetermined number of clock cycles. Yet this is exactly the same teaching that has been cited as corresponding to the device inactive decoder. Therefore, according to the Office Action, both the "device inactive decoder" and the "stabilization detective device" correspond to the same circuitry, *i.e.*, circuitry that activates the DLL for short period when transitioning from the self refresh mode to the standby mode. It is therefore clear that the Ryu *et al.* patent does not disclose or suggests any circuitry that provides a signal when the disclosed memory device is stable after reacting to a command applied to the device. Nor does the Ryu *et al.* patent disclose or suggest locking the delay interval of a DLL only when the DLL is not needed *and* a device containing the DLL has stabilized after reacting to a command.

Turning, now, to the claims, claim 1 is directed to a delay locked loop control for a delay locked loop associated with a device, such as a memory device, responding to a system clock. The control includes a device inactive decoder that provides a device inactive signal when the delay locked loop need not continue adjusting a delay interval to synchronize the system clock. As explained above, the Ryu *et al.* patent does not disclose any circuitry that performs this function. Instead, the Ryu *et al.* patent discloses circuitry that produces a signal when transitioning from one inactive mode to another inactive mode. The delay locked loop control of claim 1 also includes a stabilization detection device that provides a stabilization signal when the device is stable after reacting to a command applied to the device. As also explained above, the

Ryu *et al.* patent does not provide this teaching. Finally, the claimed control includes a delay lock for locking the delay interval on receiving both the device inactive signal and the stabilization detection signal. Again, the Ryu *et al.* patent does not disclose any circuitry that performs this function. Instead, the Ryu *et al.* patent discloses a circuit that performs its function in response to a single operating condition, namely a transition from the self refresh mode to the inactive mode. When this single condition is detected, an already locked delay interval is unlocked for a predetermined period or predetermined number of clock cycles, and the delay interval is again locked. Clearly claim 1 is not anticipated by the Ryu *et al.* patent.

Claim 15 is directed to a DRAM device containing the delay locked loop control of claim 1, and claim 22 is directed to a computer system containing the DRAM device of claim 15. These claims are therefore novel for at least the same reasons that claim 1 is novel in view of the Ryu *et al.* patent.

Claim 8 is directed to a delay locked loop control for a delay locked loop associated with a device responding to a system clock. The control includes a device inactive decoder providing a device inactive signal when data will not be read from or written to the device. The control also includes a delay lock for locking a stable delay interval on receiving the device inactive signal. As explained above with reference to claim 1, the Ryu *et al.* does not disclose a device inactive decoder providing a device inactive signal when data will not be read from or written to a device. Instead, the Ryu *et al.* teaches a circuit that produces a signal when transitioning from a first inactive mode, *i.e.*, a self refresh mode, to a second inactive mode, *i.e.*, a standby mode. Claim 8 is therefore novel over the Ryu *et al.* patent.

Claim 29 is directed to a method for saving power in a delay locked loop associated with a device responding to a system clock. The method includes determining when it is unnecessary for the delay locked loop to adjust a delay interval to synchronize with the system clock. The method also includes allowing the device to stabilize after receiving a command applied to the device before it was determined it is unnecessary for the delay locked loop to adjust the delay interval. Finally, the method includes locking the delay interval when it is unnecessary for the delay locked loop to adjust the delay interval and the device has stabilized. As explained above, the Ryu *et al.* patent does not disclose locking a delay interval after detecting both of two separate operating conditions, namely when it is unnecessary for the delay locked loop to adjust the delay interval *and* the device has stabilized after receiving a command.

The final independent claim is claim 36, which is directed to a method for saving power in a delay locked loop associated with a device responding to a system clock. The method includes determining when it is unnecessary for the delay locked loop to adjust a delay interval to synchronize with the system clock, and then locking a stable delay interval when it is unnecessary for the delay locked loop to adjust the delay interval. As explained above, the Ryu *et al.* patent does not disclose either of these acts.

The claims dependent on the above-discussed independent claims are also novel and unobvious over the Ryu *et al.* patent because of their dependency on patentable independent claims and because of the additional limitations added by those claims.

Finally, applicant is obviating the Section 112 rejection by amending claims 5 and 6 to provide missing antecedents, and applicant is amending the Title to make it more descriptive.

All of the claims in the application, *i.e.* claims 1-42, are clearly allowable. Favorable consideration and a timely Notice of Allowance are therefore earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Edward W Bulchis

Edward W. Bulchis
Registration No. 26,847
Telephone No. (206) 903-8785

EWB:dms

Enclosures:
- Postcard
- Check
- Fee Transmittal Sheet (+copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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